REMARKS

Claims 1-3 and 11 are cancelled without prejudice. Claims 4, 5 and 7-10 are presently pending and stand rejected. Claim 12 is added.

Claim 4 is amended to recite, among other limitations, "dual memory controllers, the dual memory controllers including a first memory controller and a second memory controller, the memory request arbiter including a first arbiter coupled to the first memory controller and a second arbiter coupled to the second memory controller, wherein the first arbiter and the second arbiter perform real time scheduling of memory requests, wherein memory requests to the memory shared by the plurality of devices are routed to a particular one of the first arbiter and the second arbiter based on the address of the memore request".

Examiner has indicated that Ben-Yoseph and Robinson do not teach a first and second memory controller coupled to a first and second arbiter. Examiner has indicated that Ottinger teaches "dual memory controllers (figure 1), the dual memory controllers including a first memory controller (24a, figure 1) and a second memory controller (24b, figure 1), the memory request arbiter including a first arbiter (59A, figure 2) coupled to the first memory controller and a second arbiter (59B, figure 2) coupled to the second memory controller…" Office Action at 5.

However, Assignee respectfully submits that none of the foregoing, including Ottinger teaches "wherein memory requests to the memory shared by the plurality of devices are routed to a particular one of the first arbiter and the second arbiter *based on the address of the memory request*".

For example, Ottinger col. 8, lines 32-54 discuss coherency issues. The coherency issues arise because of the

possibility of requests to the same address being provided to the different memory controllers and arbiters. As a result, Assignee respectfully submits that Ottinger does not teach "wherein memory requests to the memory shared by the plurality of devices are routed to a particular one of the first arbiter and the second arbiter *based on the address of the memory request*".

Accordingly, Assignee respectfully requests that Examiner withdraw the rejection to claim 4, and its dependent claims.

Additionally, claim 10 recites, among other limitations, "a round robin server for handling low priority tasks". The Office Action indicates that Robinett "teaches a unified memory system further comprising a round robin server for handling low priority tasks (column 28, lines 20-23)." Although Robinett teaches "the processor 160 may examine the queues in a round-robin fashion", Robinett does not differentiate handline low priority tasks. Accordingly, Assignee respectfully traverses that the combination of Ben-Yoseph and Robinette teach "a round robin server *for handling low priority tasks*". Assignee respectfully requests withdrawal of the foregoing rejection.

Moreover, new claim 12 is added reciting "a round robing server for *only* handling low priority tasks". Assignee respectfully requests allowance of claim 12.

CONCLUSION

For at least the foregoing reasons, Assignee submits that each of the pending claims are now in a condition for allowance. Accordingly, Examiner is requested to pass this case to issuance.

It is believed that all monies for the actions described herein are provided with this correspondence. To the extent that additional monies are required for any of the actions requested in the correspondence, Commissioner is authorized to charge such fees and credit any overpayments to deposit account 13-0017.

Respectfully Submitted

Date: January 4, 2010

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